Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT; PLUR=YES; OP=OR			
L24	L23 same l14	5	L24
L23	l17 same storage	67	L23
L22	L21 and l1	3	L22
L21	l14 same l19	4945	L21
L20	desired adj1 format	0	L20
L19	storage or memory	812850	L19
L18	L17 same selector	9	L18
L17	multiformat or multi-format	327	L17
L16	L15 same different	23	L16
L15	L14 same selector	281	L15
L14	conver$ near3 format	17964	L14
L13	L12 same conversion	1	L13
L12	L11 same storage	24	L12
L11	format near3 selector	331	L11
L10	L9 same (storage or memory)	16	L10
L9	L4 same format same selector	37	L9
L8	L5 same selector	5	L8
L7	L2 same select$	4	L7
L6	L5 same rule	1	L6
L5	L4 same format same address	107	L5
L4	conversion adj1 circuit	12272	L4
L3	L2 same conver$	9	L3
L2	L1 same format	22	L2
L1	scrambling adj1 circuit	191	L1

END OF SEARCH HISTORY

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Terms	Documents
5410677[uref]	10

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L7

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DATE: Wednesday, June 11, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,PGPB,JPAB,EPAB; PLUR=YES; OP=OR			
L7	5410677[uref]	10	L7
L6	L5 same circuit	42	L6
L5	l1 same l2 same selector	103	L5
L4	L3 same l1	25	L4
L3	L2 same ad	11363	L3
L2	conver$	1677893	L2
L1	storage same format	34840	L1

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L7: Entry 10 of 10 File: USPT Aug 27, 1996

US-PAT-NO: 5550987
DOCUMENT-IDENTIFIER: US 5550987 A

TITLE: Data transfer device

DATE-ISSUED: August 27, 1996

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Tanaka; Koichi	Kanagawa-ken			JP

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Kabushiki Kaisha Toshiba	Kawasaki			JP	03

APPL-NO: 08/ 097219 [PALM]
DATE FILED: July 27, 1993

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
JP	4-201392	July 28, 1992

INT-CL: [06] G06 F 13/38

US-CL-ISSUED: 395/286; 395/280
US-CL-CURRENT: 710/106; 710/100

FIELD-OF-SEARCH: 395/325, 395/425, 395/775, 395/550, 395/500, 395/275

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

Search Selected | Search ALL

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
☐	3226693	December 1965	Dumey	395/550
☐	4837571	June 1989	Lutz	341/67
☐	4959779	September 1990	Weber et al.	395/775
☐	5243699	September 1993	Nickolls et al.	395/275
☐	5251312	October 1993	Sodos	395/425
☐	5265259	November 1993	Satou et al.	395/325
☐	5341508	August 1994	Keeley et al.	395/325
☐	5398328	March 1995	Weber et al.	395/425
☐	5410677	April 1995	Roskowski et al.	395/500

FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
63-263524	October 1988	JP	
2-141857	May 1990	JP	
3-160550	July 1991	JP	

ART-UNIT: 235

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Wiley; David A.

ATTY-AGENT-FIRM: Foley & Lardner

ABSTRACT:

A data transfer device has a input circuit for receiving a data block of a data structure including data elements of different lengths in each set data length from a transfer source, a converter for assembling data received by the input circuit into data elements and converting the structure of the assembled data elements to endian format for a memory, an output circuit for providing to a memory, data elements which have been structurally converted by the converter for each set data length. The device further has a first register for storing a data structure for transmitted data blocks, a second register for storing transfer source endians and transfer destination endians, and a controller for controlling the assembly process for the converter according to the data structure stored in the first register, for controlling the conversion process for the converter according to endian formats stored in the second register, and for controlling the input and output of data for the input circuit and for the output circuit.

28 Claims, 16 Drawing figures

WEST

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L6: Entry 11 of 42 File: USPT Apr 25, 1995

DOCUMENT-IDENTIFIER: US 5410677 A
TITLE: Apparatus for translating data formats starting at an arbitrary byte position

CLAIMS:

6. A circuit for translating data in one of a plurality of data formats into data in any of the other of the plurality of the data formats as claimed in claim 1 in which the first storage device comprises a first register having a number of bit positions equal to the number of bits in the largest format to be converted and capable of storing bits in sequential order as they are received; and the first selector comprises a second register having a number of bit positions equal to the number of bits in the largest format to be converted and capable of storing bits in sequential order as they are received, and a multiplexor for selecting data from the first and the second registers.

8. A circuit for translating data in one of a plurality of data formats into data in any of the other of the plurality of the data formats as claimed in claim 1 in which the first storage device comprises a first register having a number of bit positions equal to the number of bits in the largest format to be converted and capable of storing bits in sequential order as they are received; and the first selector comprises a second register having a number of bit positions equal to the number of bits in the largest format to be converted and capable of storing bits in sequential order as they are received, and a multiplexor for selecting data from the first and the second registers.

10. A circuit for translating data in one of a plurality of data formats into data in any of the other of the plurality of the data formats as claimed in claim 1 in which the first storage device comprises a first register having a number of bit positions equal to the number of bits in the largest format to be converted and capable of storing bits in sequential order as they are received; and the first selector comprises a second register having a number of bit positions equal to the number of bits in the largest format to be converted and capable of storing bits in sequential order as they are received, and a multiplexor for selecting data from the first and the second registers.

12. A circuit for translating data in one of a plurality of data formats into data in any of the other of the plurality of the data formats as claimed in claim 1 in which the first storage device comprises a first register having a number of bit positions equal to the number of bits in the largest format to be converted and capable of storing bits in sequential order as they are received; and the first selector comprises a second register having a number of bit positions equal to the number of bits in the largest format to be converted and capable of storing bits in sequential order as they are received, and a multiplexor for selecting data from the first and the second registers.

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End of Result Set

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L6: Entry 42 of 42 File: EPAB Nov 21, 1991

DOCUMENT-IDENTIFIER: EP 457039 A2
TITLE: Pixel-depth converter for a computer video display.

Abstract Text (1):
A pixel-depth converter for converting source-pixel data having a source-pixel depth to destination-pixel data having a destination-pixel depth which differs from the source-pixel depth by a user-selectable pixel-depth-conversion scale factor includes a packed-pixel-data depacker circuit, a pixel-data-conversion-table storage circuit and a plurality of conversion-table address-selector multiplexers. The packed-pixel-data depacker circuit receives source-pixel data words having a packed-pixel data format from a source-pixel-data memory and transmits the data words depacked-pixel-data-word-component-by-depacked-pixel-data-word-component in accordance with the selected pixel-depth-conversion scale factor. The pixel-data-conversion-table storage circuit stores user-selectable depth-altering pixel-data-conversion data in locations having conversion-table read addresses which are associated with values of depacked-source-pixel-data portions corresponding to the selected pixel-depth-conversion scale factor. The pixel-data-conversion-table storage circuit includes a plurality of independently-operable converted-data-read parallel output ports and a like plurality of associated conversion-table read-address input ports. Depacked-source-pixel-data-portion conversion-lookup addresses may be applied independently in parallel to the plurality of conversion-table read-address input ports of the pixel-data-conversion-table storage circuit and pixel-data-conversion data stored in locations specified by the addresses can be read in parallel from the associated converted-data-read parallel output ports. Each conversion-table address-selector multiplexer has a plurality of depacked-source-pixel-data-portion input ports, a conversion-lookup address output port and an address-selector-multiplexer control-signal input port. The depacked-source-pixel-data-portion input ports of each address-selector multiplexer are connected respectively to corresponding terminal subsets of the depacker circuit which are associated with different pixel-depth-conversion scale factors. The conversion-lookup address output port of each of the conversion-table address-selector multiplexers is connected to an associated read-address input port of the pixel-data-conversion-table storage circuit. Finally, the address-selector-multiplexer control-signal input ports are connectable to a scale-factor-selection signal bus for receiving a scale-factor-selection signal which specifies the desired pixel-depth-conversion scale factor and corresponding depacked-source-pixel-data portions to serve as depacked-source-pixel-data-portion conversion-lookup addresses.

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Terms	Documents
L5 same circuit	42

Database: US Patents Full-Text Database; US Pre-Grant Publication Full-Text Database; JPO Abstracts Database; EPO Abstracts Database; Derwent World Patents Index; IBM Technical Disclosure Bulletins

Search: L6

Refine Search

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Search History

DATE: Wednesday, June 11, 2003 Printable Copy Create Case

Set Name side by side	Query	Hit Count	Set Name result set
DB=USPT,PGPB,JPAB,EPAB; PLUR=YES; OP=OR			
L6	L5 same circuit	42	L6
L5	l1 same l2 same selector	103	L5
L4	L3 same l1	25	L4
L3	L2 same ad	11363	L3
L2	conver$	1677893	L2
L1	storage same format	34840	L1

END OF SEARCH HISTORY

WEST

Generate Collection Print

L12: Entry 15 of 24 File: USPT Apr 25, 1995

DOCUMENT-IDENTIFIER: US 5410677 A
TITLE: Apparatus for translating data formats starting at an arbitrary byte position

CLAIMS:

16. A circuit for translating data in one of a plurality of data formats into data in any of the other of the plurality of the data formats comprising a first channel including a storage device for storing data appearing in a first format in groups each equal to the number of bytes of data in a second format, a selector coupled to said storage device and selecting unused bytes from a first one of the groups stored by the storage device and from a second one of the groups stored by the storage device, a first rotator coupled to said selector and placing the unused bytes selected in numerical byte order according to the number of transfers already made, a second rotator coupled to said first rotator and placing the data in the numerical byte order in an arbitrary byte position for transfer to the format of a destination device, and a counter coupled to said selector and determining the number of bytes utilized in the format to which the data is to be translated and the number of transfers already made.

WEST

Generate Collection Print

L3: Entry 4 of 9 File: USPT Jul 27, 1993

DOCUMENT-IDENTIFIER: US 5231667 A
TITLE: Scrambling/descrambling circuit

Detailed Description Text (44):
Conventionally, processing circuits 11 (11a through 11h) on the transmitting side process eight-bit data in parallel and send the processed data to a parallel-to-serial conversion circuit 12 for conversion to serial data. The output of the parallel-to-serial conversion circuit 12 is scrambled by a scrambling circuit 13, the scrambled data being placed onto a transmission line. On the receiving side, a descrambling circuit 14 descrambles the data coming over the transmission line. The output of the descrambling circuit 14 is converted by a serial-to-parallel conversion circuit 15 to parallel data for processing by processing circuits 16 (16a through 16h). Because the processing circuits 11 and 16 need only operate at one-eighth of the bit transmission rate, they may be manufactured in LSI format as a low-speed, inexpensive CMOS arrangement. With the prior art, however, the parallel-to-serial conversion circuit 12, serial-to-parallel conversion circuit 15, scrambling circuit 13 and descrambling circuit 14 must be constructed discretely in a highspeed, expensive ECL arrangement each.

Detailed Description Text (45):
By contrast, the scrambling/descrambling circuit embodying the invention may operate at low speed because it processes eight bits in parallel. Thus the processing circuits 11, scrambling circuit 17, processing circuits 16 and descrambling circuit 20 can be manufactured in LSI format as a CMOS arrangement. Only the parallel-to-serial conversion circuit 18 and serial-to-parallel conversion circuit 19 need to be constructed as an ECL arrangement that operates at high speed.

Detailed Description Text (46):
Thus according to the invention, the data processed by the processing circuits 11 on the transmitting side are scrambled by the scrambling circuit 17, followed by conversion from parallel to serial format. On the receiving side, the data are converted from serial to parallel format before being descrambled.

WEST

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L3: Entry 7 of 9 File: USPT Nov 3, 1992

DOCUMENT-IDENTIFIER: US 5161187 A
TITLE: Cable television system

Detailed Description Text (5):
The transmitting station 1 includes a television signal generator 4, a scrambling circuit 5, and a transmitter 6. The television signal generator 4 generates a television signal of a standard format. Then, the television signal is converted by the scrambling circuit 5 into a corresponding television signal of a special format, that is, a corresponding scrambled television signal. The transmitter 6 generates an SHF-band television signal from the scrambled television signal through a suitable process such as a frequency modulation process using a carrier signal, and transmits the SHF-band television signal to the communication satellite 3 via an antenna 7.

Detailed Description Text (7):
The receiving station 2 includes a converter 9, a de-scrambling circuit 10, and a television receiver 11. The receiving station 2 receives the SHF-band television signal from the communication satellite 3 via an antenna 8. The received SHF-band television signal is converted by the converter 9 into a corresponding down-converted television signal (a corresponding UHF-band or VHF-band television signal) through a suitable process such as an FM demodulation process. The down-converted television signal is subjected by the de-scrambling circuit 10 to a conversion inverse with respect to the conversion by the scrambling circuit 5 in the transmitting station 1, so that the original standard-format television signal is restored from the down-converted television signal. The restored standard-format television signal is fed to the television receiver 11, and the video and audio information represented by the standard-format television signal is reproduced by the television receiver 11.

Detailed Description Text (9):
In the transmitting station 1, the standard-format television signal generated by the television signal generator 4 has a waveform such as shown in FIG. 2. The scrambling circuit 5 processes and converts the standard-format television signal into the special-format television signal which has a waveform such as shown in FIG. 3. Specifically, the scrambling circuit 5 removes a serrated vertical sync pulse and adjacent equalizing pulses from the standard-format television signal, and adds an identification signal (an ID signal) to the standard-format television signal at a predetermined position within a vertical blanking period. The ID signal is composed of predetermined codes.

Detailed Description Text (11):
As shown in FIG. 5, the de-scrambling circuit 10 in the receiving station 2 includes a tuner 19 selects a signal of a desired frequency channel from the output VHF-band or UHF-band television signal of the converter 9. The selected television signal is subjected by a detector 20 to video detection. The selected channel is designated by a channel selector within a terminal controller 21. The terminal controller 21 also has a section for generating a reference signal of codes equal to the codes composing the ID signal in the transmitting station 1. The reference signal generating section of the terminal controller 21 is formed by using a suitable device such as a magnetic card or a ROM. An ID signal detector 22 detects an ID signal from an output signal of the video detector 20 by using a suitable device such as a shift register. A comparator 23 compares the detected ID signal with the reference signal generated by the terminal controller 21, and generates an agreement signal when the detected ID signal agrees with the reference signal. A sync separator 24 separates a horizontal sync signal from the output signal of the video detector 20. A vertical sync signal generator 25 generates a vertical sync signal on the basis of the separated horizontal sync signal, the vertical sync signal being equivalent to the vertical sync signal of the standard-format television signal. The timing of the generation of the vertical sync

signal is determined by the agreement signal fed from the comparator 23 so that the vertical sync signal will occur at a time position equal to the time position of the vertical sync signal of the standard-format television signal. A vertical sync signal inserting circuit 26 adds the generated vertical sync signal into the output signal of the video detector 20, recovering the standard-format television signal (see FIG. 2). An RF modulator 27 modulates the carrier signal of a given frequency channel with the standard-television signal, converting the standard-format television signal into a corresponding RF television signal which is fed to the television receiver 11. A calculator 28 calculates the charge in response to a channel designating signal outputted from the terminal controller 21, and the agreement signal outputted from the comparator 23. Data representing the calculated charge are printed on a sheet or stored into a memory.

WEST

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L12: Entry 16 of 24 File: USPT Jul 5, 1994

DOCUMENT-IDENTIFIER: US 5327076 A
TITLE: Glitchless test signal generator

CLAIMS:

1. A test signal generating system for generating glitchless test signals to be provided to an electronic circuit component under test in a burn-in system, the test signal generating system comprising:

a data generator providing a data signal;

a timing generator providing a cycle clock signal;

a format selector providing a format signal;

a trigger clock providing a trigger clock signal formed of pulses and having trigger clock period;

first storage means, connected to the data generator, the timing generator, the format selector and the trigger clock, for storing as stored signals the present states of the data signal, the cycle clock signal and the format signal upon receipt of one of the pulses in the trigger clock signal;

test signal selection means, coupled to the first storage means, for receiving the stored signals and providing a test signal based on the stored signals;

second storage means, coupled to the test signal selection means and the trigger clock, for storing as a stored test signal a present state of the test signal upon receipt of a pulse in the trigger clock signal; and

wherein the second storage means provides the stored test signal until a subsequent pulse in the trigger clock signal such that glitches in the test signal caused by skew in timing of providing the stored signals to the test signal selection means are not passed to the electronic circuit component under test.

3. The system of claim 2 wherein the first storage means comprises a first flip-flop electrically connected to an output of the data generator and a first input of the test signal selection means, a second flip-flop electrically connected to an output of the timing generator and a second input of the test signal selection means, and a third flip-flop electrically connected to an output of the format selector and a third input of the test signal selection means, and wherein the second storage means comprises a fourth flip-flop electrically connected to the output of the test signal selection means.

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L16: Entry 7 of 23 File: USPT Dec 1, 1998

DOCUMENT-IDENTIFIER: US 5844629 A
TITLE: Digital-to-analog video encoder with novel equalization

Detailed Description Text (11):
Preferably, matrix converter 60 is provided with a format selector input 64 which may be used to control the CAV output format and the respective conversion algorithm. For example, the matrix converter 60 may be switched between the RGB and the Y/PR/PB formats using a single format selector line 64. Although several slightly different Y/PR/PB formats exist, the following set of scaling factors is one example being used in studio equipment.

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L24: Entry 4 of 5 File: USPT Sep 24, 1996

DOCUMENT-IDENTIFIER: US 5559954 A
TITLE: Method & apparatus for displaying pixels from a multi-format frame buffer

CLAIMS:

1. An apparatus for displaying a plurality of pixels on a display monitor, said apparatus comprising:

multi-format pixel storage means for storing said plurality of pixels, each pixel comprising one of a plurality of pixel format types;

first pixel map storage means for storing a format pixel map comprising a plurality of format identifiers, wherein said format identifiers specify a pixel format type for a corresponding pixel;

conversion means coupled to said multi-format pixel storage means for converting a pixel to a display compatible pixel for each format type to generate a plurality of display compatible pixels;

second pixel map storage means coupled to said first pixel map storage means for said format pixel map for rendering pixels for display on said display monitor; and

transferring means coupled to said first pixel map storage means and second pixel map storage means for transferring said format pixel map from said first pixel map storage means to said second pixel map storage means during a pre-determined interval, and for transferring a format identifier from said format pixel map to said second pixel map storage means for selection of said display compatible pixel; and

selection means coupled to said conversion means and said second pixel map storage means for selecting a display compatible pixel from said plurality of display compatible pixels based on a corresponding format identifier from said format pixel map such that said display compatible pixel selected is compatible for display on said display monitor.

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